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09/607,783	06/30/2000	Brian K. Holscher	042390.P8839	9530

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,783	HOLSCHER, BRIAN K.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-10 and 13-18* is/are rejected.

7)☒ Claim(s) *3,4,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of Applicant's amendment to the title the objection has been withdrawn.

2. In view of Applicant's amendment to claim 11 the objection has been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claims recite the negative limitation "wherein the second input is not directly coupled to an adjacent one of the computational cells", while the limitation is not present in the specification as filed. The mere absence of a positive recitation is not basis for exclusion. This use of negative limitations is improper according to Negative Limitations section in the MPEP. See MPEP §2173.05(i).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen et al, U.S. Patent Number 4,510,581 (herein referred to as Cohen).

5. Referring to claim 13 Cohen has taught a method comprising:

determining an availability vector corresponding to an availability status of buffers in an array of buffers (Cohen abstract figures 2 and 5 column 1 lines 44-56);

determining a current selected entry vector that identifies a most recently allocated buffer (Cohen figures 2 and 5 reference number 32 from the previous cell, column 5 lines 37-61; the second input shows which of the buffers are being selected, and then that information is passed on to the next cell so that it knows that the previous buffer has been allocated and filled); and

determining a next available buffer vector that identifies the next available buffer to be allocated from among the plurality of buffers as a function of the availability vector and the current selected entry vector (Cohen figures 2 and 5, reference number 74, column 5 lines 37-47).

6. Referring to claim 14 Cohen has taught wherein the array of buffers comprises N buffers and the availability vector comprises N bits, each bit corresponding to an availability status of a respective buffer (Cohen figures 2 and 5 reference number 28, column 3 lines 46-50).

7. Referring to claim 15 Cohen has taught wherein the array of buffers comprises N buffers and the current selected entry vector comprises N bits, each bit corresponding to a respective buffer, said current selected entry vector including only one bit that is asserted, said asserted bit identifying a most recently allocated buffer (Cohen figures 2 and 5 reference number 32 from the previous cell, column 5 lines 37-61).

8. Referring to claim 16 Cohen has taught wherein the array of buffers comprises N buffers and the next available buffer vector comprises N bits, each bit corresponding to a respective buffer, said next available buffer vector including only one bit that is asserted, said asserted bit identifying a next available buffer to be allocated (Cohen figures 2 and 5 reference number 32 from the previous cell, column 5 lines 19-61; only one buffer is filled at a time).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-2 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen in view of John Wakerly, Digital Design, Principles and Practice (referred to herein as Wakerly).

10. Referring to claim 1 Cohen has taught an apparatus comprising:

an array of computational cells coupled to one another and having a one-to-one correspondence with respective buffers of an array of buffers (Cohen figures 2 and 5, reference number 28, abstract column 1 lines 44-56; the selection circuit 12 and block 70 are looked at as a single cell as described by the claims), wherein each computational cell includes:

a first input for receiving data corresponding to an availability status of the respective buffer corresponding to the computational cell (Cohen figures 2 and 5 reference number 28, column 3 lines 46-50);

a second input for receiving data corresponding to a currently selected buffer from among the array of buffers (Cohen figures 2 and 5 reference number 30 from the previous cell, column 5 lines 37-61; the second input shows which of the buffers are being selected, and then that information is passed on to the next cell so that it knows that the previous buffer has been allocated and filled)

a first output upon which data is produced for identifying a next available buffer,

a third input (Cohen figures 2 and 5 reference number 32 of the previous selection unit); and

a second output coupled to the third input of a next computational cell (Cohen figures 2 and 5 reference number 30 column 3 lines 9-32);

wherein the data produced on the first outputs of the computational cells collectively comprise a next available buffer vector that identifies a next buffer in the buffer array to be allocated (Cohen figures 2 and 5, reference number 74, column 5 lines 37-47).

11. Cohen has not explicitly taught:

wherein the first output is coupled to logically AND the first input with the third input.

Cohen has taught that the line 32 of figure 5 corresponds with line 28, which relates to the first input, such that when 28 goes high, 32 is also a logical true (Cohen column 3 lines 46-50). Cohen has also taught where logic block 70 is a flip flop, wherein 32, which corresponds directly to the first input 28 as shown above, and the 32 of the previous selection circuit, which corresponds as the third input, are both inputs into the flip-flop (Cohen column 5 lines 21-36).

Wakerly has taught:

wherein the first output is coupled to logically AND the first input with the third input (Wakerly page 543, figure 7-21; the input D and the enable are logically ANDed through the AND gate). Since Cohen does not give the details of the flip-flop 70, one of ordinary skill in the art at the time of the invention would have been motivated to find the logical gates used in a flip-flop with an enabling input. As taught by Cohen, the third input is the enabling input, and the first input 28 corresponds to line 32 is the other input of the flip-flop. Although other configurations exist for flip-flops with two inputs, they all will contain a LOGICAL AND. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to look to Wakerly for the details of the flip-flop to be able to do a detailed design of Cohen.

12. Referring to claim 2 Cohen has taught wherein each computational cell further comprises:

data is produced on the second output of a given computational cell as a function of data received at the first, second, and third inputs for the computational cell (Cohen figures 2 and 5 reference number 30 column 3 lines 9-32).

13. Referring to claim 6 Cohen has taught wherein the array of buffers comprises N buffers (Cohen figure 5) and data received at the first input of each computational cell collectively comprise an availability vector comprising N bits, each bit corresponding to an availability status of a respective buffer (Cohen figures 2 and 5 reference number 28, column 3 lines 46-50).

14. Referring to claim 7 Cohen has taught wherein the array of buffers comprises N buffers (Cohen figure 5) and data received at the second input of each computational cell collectively comprise a current selected entry vector comprising N bits, each bit corresponding to a

respective buffer, said current selected entry vector including only one bit that is asserted, said asserted bit identifying a most recently allocated buffer (Cohen figures 2 and 5 reference number 32 from the previous cell, column 5 lines 37-61).

15. Referring to claim 8 Cohen has taught wherein the array of buffers comprises N buffers (Cohen figure 5) and the next available buffer vector comprises N bits, each bit corresponding to a respective buffer, said next available buffer vector including only one bit that is asserted, said asserted bit identifying the next available buffer to be allocated (Cohen figures 2 and 5 reference number 32 from the previous cell, column 5 lines 19-61; only one buffer is filled at a time).

16. Referring to claim 9 Cohen has taught a processor comprising:

an array of buffers (Cohen figure 5 abstract);

an array of computational cells coupled to one another in a cascaded fashion, each computational cell corresponding to a respective buffer in the array of buffers (Cohen figures 2 and 5, reference number 28, abstract column 1 lines 44-56; the selection circuit 12 and block 70 are looked at as a single cell as described by the claims) and including:

a first input for receiving data corresponding to an availability status of a buffer corresponding to the computational cell (Cohen figures 2 and 5 reference number 28, column 3 lines 46-50);

a second input for receiving data corresponding to a currently selected buffer from among the array of buffers (Cohen figures 2 and 5 reference number 30 from the previous cell, column 5 lines 37-61; the second input shows which of the buffers are being selected, and then that information is passed on to the next cell so that it knows that the previous buffer has been allocated and filled);

a first output upon which data is produced for identifying a next available buffer (Cohen figures 2 and 5, reference number 74, column 5 lines 37-47); and

a second output (Cohen figure 2 and 5);

a third input (Cohen figures 2 and 5 reference number 32 of the previous selection unit), coupled to the second output of a preceding computational cell, wherein the data produced on the first outputs of the computational cells collectively comprise a next available buffer vector that identifies the next buffer in the buffer array to be allocated for use (Cohen figures 2 and 5 reference number 30 column 3 lines 9-32).

17. Cohen has not explicitly taught:

wherein the first output is coupled to logically AND the first input with the third input.

Cohen has taught that the line 32 of figure 5 corresponds with line 28, which relates to the first input, such that when 28 goes high, 32 is also a logical true (Cohen column 3 lines 46-50). Cohen has also taught where logic block 70 is a flip flop, wherein 32, which corresponds directly to the first input 28 as shown above, and the 32 of the previous selection circuit, which corresponds as the third input, are both inputs into the flip-flop (Cohen column 5 lines 21-36).

Wakerly has taught:

wherein the first output is coupled to logically AND the first input with the third input (Wakerly page 543, figure 7-21; the input D and the enable are logically ANDed through the AND gate). Since Cohen does not give the details of the flip-flop 70, one of ordinary skill in the art at the time of the invention would have been motivated to find the logical gates used in a flip-flop with an enabling input. As taught by Cohen, the third input is the enabling input, and the first input 28 corresponds to line 32 is the other input of the flip-flop. Although other configurations exist for

flip-flops with two inputs, they all will contain a LOGICAL AND. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to look to Wakerly for the details of the flip-flop to be able to do a detailed design of Cohen.

18. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen in view of Garibay, Jr. et al, U.S. Patent Number 6,219,773 (herein referred to as Garibay).

19. Referring to claims 5 and 10 Cohen has taught wherein a plurality of computational cells are arranged in a cascaded order so as to define 0^{th} to N^{th} computational cells such that the second output from an it" computational cell is coupled to the third input of an (I^n + 1) computational cell (Cohen figures 2 and 5). Cohen has not taught the second output from the N^{th} computational cell is coupled to the third input of the 0^{th} computational cell. Garibay has taught using a circular buffer (Garibay column 12 lines 21-37). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Cohen and Garibay so that the system of Cohen could operate as a circular buffer allocation circuit. By having the last entry of the buffer wraparound to the first entry of the buffer, the oldest entry which has already been used in the buffer is written over and the buffer seems to continue on forever, since the buffer wraps around, allowing more entries to be added to the buffer. The same is true in allocating buffer circuits since by wrapping around the information that the last buffer in the array was allocated last, the first buffer in the array knows it will be next, so the process dos not stop, and buffers and continually allocated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to allow the buffer selection circuits to wraparound, so that the allocation process would not stop after the last buffer is allocated.

20. Referring to claims 17 and 18 Cohen has taught wherein the second input is not directly coupled to an adjacent one of the computational cells (Cohen figure 2; as seen in figure 2, the output of one selection circuit 30 is not the same as the input into the next selection since it is split and enters the next selection circuit is input 18).

Allowable Subject Matter

21. Claims 3-4 and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. Referring to claims 3-4 and 11-12 Cohen and Garibay has not taught individually, or in combination, wherein each computational cell comprises an inverter for receiving data on the first input of the cell and having an output, a first AND gate having a first input coupled to the output of the inverter, a second input for receiving data on the third input of the cell, and having an output, a second AND gate, having a first input for receiving data on the first input of the cell and a second input for receiving data on the third input of the cell, said second AND gate having an output corresponding to the first output of the cell, an OR gate, having a first input coupled to the output of the first and gate, and a second input for receiving the data on the second input of the cell, said OR gate having an output corresponding to the second output of the cell.

Response to Arguments

23. Applicant's arguments in paper numbers 3 and 4 with respect to claims 1-12 filed on 03/15/04 have been considered but are moot in view of the new ground(s) of rejection.

24. Applicant's arguments in paper numbers 3 and 4 with respect to claims 13-16 filed on 03/15/04 have been considered but they are not persuasive.

25. In the remarks, in regard to the rejection of claims, Applicant argues in essence that:

"Applicants respectfully submit that Cohen fails to disclose determining an availability vector corresponding to an availability status of each buffer."

26. This is not persuasive. Cohen shows each selection circuit 1-n in figure 5 receiving a separate availability signal, or clear pulse, 28a-n. A vector is simply a one-dimensional array in computer architecture. In this case, the availability signals of Cohen would make up a vector of availability bits together, one element of the vector for each selection circuit.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

May 27, 2004